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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,280	05/30/2001	Mojdeh Shakeri	MWS-040RCE	7303
74321 7590 02/20/2008 LAHIVE & COCKFIELD, LLP/THE MATHWORKS One Post Office Square Boston, MA 02109-2127			EXAMINER STEVENS, THOMAS H	
			ART UNIT	PAPER NUMBER
			2121	
			MAIL DATE	DELIVERY MODE
			02/20/2008	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 09/870,280	<b>Applicant(s)</b> SHAKERI ET AL.	
	<b>Examiner</b> Thomas H. Stevens	<b>Art Unit</b> 2121	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 16 January 2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,2,4-9 and 11-37 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-9,11-16,18-37 is/are rejected.
- 7) ☒ Claim(s) 17 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

1. Claims 1,2,4-9,11-37 were examined.

### *Section I: Final Rejection*

#### **Claim Interpretation**

2. Office personnel are to give claims their "**broadest reasonable interpretation**" in light of the supporting disclosure. *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997): Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See \*also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow") .... The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed .... An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process. Pg. 7 of the disclosure (05/30/2001) defines attributes as the following:

*A composite signal represents an ordered set of signals that are bundled together to form a single entity. **Signals in a composite signal can have different attributes, i.e., data types, numeric types, dimensionalities, and so forth.** Therefore, the composite signal is a general facility for grouping and splitting a set of heterogeneous or homogeneous signals without loss of information.*

3. Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-7, 11-14, 18-26, 28-36 are rejected under 35 U.S.C. 103(a) as being unpatentable by Dwan et al., titled, "Introducing Simulink into a Systems Engineering Curriculum" (1993); hereafter Dwan, in view of Jantsch et al., titled, "Composite Signal Flow: A computational model combining sampled streams, and vectors" hereafter Jantsch.

**Per claims 1, 11,12,14,21,25,29,33-36 Dwan teaches**

- modeling process (i.e., simulation, pg. 627, Preliminaries section)
- providing a plurality of blocks (the teaching of manipulating a plurality of blocks, pg.627, "To Manipulate Blocks" section paragraphs 1-3)
- generating a plurality of output signal values ("plot your results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results" section, 1st paragraph) (pg.628, right column, "To interconnect the blocks" section) from the plurality of blocks (the teaching of manipulating a plurality of blocks, pg.627, "To Manipulate Blocks" section paragraphs 1-3)
- grouping the plurality of output signals ("plot your results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results" section, 1st paragraph) (pg.628, right column, "To interconnect the blocks" section)
- as an ordered set in a multiplexer (pg.628, right column, "To interconnect the blocks" section, "mux")
- in a storage device (inherency since software is stored on a disk, computer etc.).

**but Dwan fails to teach each storing and outputting and output signal having at least one attribute and the first composite signal preserving the at least one attribute of each output signal to which Jantsch teaches**

- storing, and outputting, each output signal having at least one attribute (see claim interpretation with pg.159, figure 8, signals)

- the first composite signal preserving the at least one attribute(see claim interpretation with pg.159, figure 8, signals, the attribute of  $[t, v'_0, v'_1]$  is still preserved to the right of A) of each output signal
- blocks representing functional entities operate on a plurality of input signal values (pg. 158, figure 4, "The composite signal model implemented in SDL and MATLAB)

Therefore at the time of invention, it would have been obvious to one of ordinary skill in the art to modify Dwan by Jantsch because Jantsch teaches a method to provide a relatively simple, formally sound model of computation, which can be the basis for heterogeneous modeling and simulation environments (pg. 154, right column, 2<sup>nd</sup> paragraph, lines 1-4)

**Per clam 2, Jantsch teaches**

- Blocks includes at least one output signal port (example of a composite block to which the user has the ability to duplicate this composite block, pg.158, figure 5)

**Per claims 4,32 Dwan teaches**

- attribute is a name (pg.627, left column, "The Windows Environment" section, point 3, 'click on the title block of the window"; pg.630, figure 4, "clock").

**Per claim 5 Dwan teaches**

- attribute is a data type (example, pg.630, figure 3, "transfer form") .

**Per claim 6, Dwan teaches**

- attribute is a numeric type (example, pg.629, right column, lines 1-10, list of numeric parameters) .

**Per claims 7,30,31 Dwan teaches**

- the attribute is a dimensionality (2 dimensional matrix, pg.630, left column, section 4b "output matrix be a (2 x 2) matrix).

**Per claims 12,18,19 Dwan teaches**

- viewing (pg.630, figure 3, "scope")

**Per claims 13,16 Jantsch teaches**

- a second composite signal (second composite signal is represented on page 159, figure 8, could represent a composite input signal of A)

**Per claim 14, Dwan teaches**

- the first and second block(covers a plurality of blocks, pg.627, right column, "To Manipulate Blocks" section, numbers 1-3);

- processing the composite signal in a third block (covers a plurality of blocks, pg.627, right column, "To Manipulate Blocks" section, numbers 1-3)

**Per claims 19, 20 Dwan teaches**

- the GUI(inherent to the Windows application, pg.627, "Windows Environment") is provided on an input/output device.

**Per claim 22 Dwan teaches**

- The computer program product of claim 21 wherein the computer readable medium is a random access memory (RAM) (inherent to the properties of a computer; pg.627, left column, "Preliminaries" 386 processor which is stored on PC).

**Per claim 23 Dwan teaches**

- read only memory (ROM) (inherent to the properties of a computer; pg.627, left column, "Preliminaries" 386 processor which is stored on PC).

**Per claim 24 Dwan teaches**

- hard disk drive(inherent to the properties of a computer; pg.627, left column, "Preliminaries" 386 processor which is stored on PC).



**Per claims 26, 28 Dwan teaches**

- the processor and the memory (inherent to the properties of a computer; pg.627, left column, "Preliminaries" 386 processor which is stored on PC) are incorporated into a personal computer.
- the processor (inherent to the properties of a computer; pg.627, left column, "Preliminaries" 386 processor which is stored on PC) and the memory are incorporated into a single board computer.

**Per claim 36, Dwan teaches**

- A method for graphically representing a composite signal in a modeling environment, (i.e., simulation, pg. 627, Preliminaries section)
- the method comprising the steps of: providing a plurality of output signals ("plot your results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results" section, 1st paragraph)
- from one or more blocks, each output signal graphically (pg.630, figure 3, "scope") indicated by a signal identifier; providing a composite signal identifier to graphically (pg.627, right column, bullet 8, "make hard copies of MATLAB plots)
- indicated a grouping of signal identifiers, the composite signal identifier representing a composite signal comprising a set of the plurality of output signals ("plot your results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results" section, 1st paragraph)
- and storing the composite signal identifier in a storage device (inherency since software is stored on a disk, computer etc.).

7. Claims 8, 9 and 15 and 27 were rejected under 35 U.S.C. 103(a) as being unpatentable over Dwan in view of Jantsch as applied to claims 1,14 and 27 above, and further in view of Austin et al.,titled, "Structure Matrix Computations with Units"; hereafter Austin. Dwan teaches most of the instant application above but fails to teach data structure data tree, network server residing in the Internet and  $m + n$  nodes.

**Austin teaches**

- Per claim 5 : list data structure (example of a row/column data structure, pg. 18, "Casting Units in Matrix Output")
- Per claims 8 and 15: a linked list data structure (pg. 25, line 15 and pg. 29, figure 11c, "Quantity Data Structure" and "Units Data Structure")
- Claim 9. the tree data structure(pg. 27, figure 10); including  $m+n$  nodes (pg. 38, lines 27 and 28 with pg. 19, "Addition and Subtraction" section).
- Claim 27: a network server residing in the Internet (pg. 2, Introduction, line 1).

Therefore, it would have been obvious to one having ordinary skill the art at the time the invention was made to utilize the Matlab software in Dwan in the data structure of

Austin because Austin teaches a solution of self-contained and established problem solving procedures, where the structure of a problem's input/output is well understood, identifying and correcting unintentional errors in the solution of new and innovative computations can be significantly easier when units are an integral part of the computation procedure (Austin: pg.3, lines 1-5).

### ***Section II: Response to Arguments***

8. Applicants are thanked for addressing these issues. The mux limitation is acknowledged however this issue is substantiated or is modified by Jantsch's composite signal model in which at least one attribute is preserved at the output as said forth above.

Furthermore, to cease prosecution, applicants are **strongly encouraged** to modify each independent claim by way of claim 17.

### ***Conclusion***

9. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the

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shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

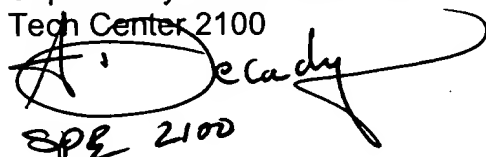
### ***Conclusion***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715.

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Albert Decady (571-272-3819). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

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